Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **Y1**
2. **A1**
3. **B1**
4. **Y2**
5. **A2**
6. **B2**
7. **GND**
8. **VCC**
9. **Y4**
10. **B4**
11. **A4**
12. **Y3**
13. **B3**
14. **A3**

**.065”**

**9 8 7 6**

**12 13 14 1 2**

**5**

**4**

**3**

**10**

**11**

**MCHCØ**

**.050”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: MCHC02**

**APPROVED BY: DK DIE SIZE .050” X .065” DATE: 3/1/16**

**MFG: MOTOROLA THICKNESS .014” P/N: 54HC02**

**DG 10.1.2**

#### Rev B, 7/1